

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	(714/741.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:36
L2	7	(714/726.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:36
L3	0	(714/717.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L4	6	(714/738.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L5	9	(714/724.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L6	0	(714/48.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:38
L7	45	(716/16.ccls.) and emulation and ((configur\$5 or program\$4) with ((logic adj block\$1) or FPGA)) and test\$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:38
S14 6	2	(inverse adj routing) with configuration	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/19 16:37
S15 1	1	inverse with routing with ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:01
S15 2	1	inverse with routing same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:01

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S15 3	19	(inverse with rout\$3) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:17
S15 4	1	(inverse adj rout\$3) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:03
S15 6	55	loopback with output with result	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 14:57
S15 8	5	(loopback with output with result) and (fail\$3 with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:02
S15 9	1	((loopback with output with result) same logic) and (fail\$3 with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:03
S16 0	48	((loopback with output) same logic) and (fail\$3 with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:07
S16 1	2	((loopback with output) same logic same (fail\$3 with indicat\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:11
S16 2	1	((loopback with output) same logic same FPGA) and (fail\$3 with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:13

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S16 3	1	((loopback with output) same FPGA) and (fail\$3 with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:14
S16 4	16	(loopback with output) and (fail\$3 with indicat\$3) and FPGA and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:20
S16 7	16	(loopback with output) and (fail\$3 with indicat\$3) and FPGA and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:27
S16 9	38	(loopback with output) and (fail\$3 with indicat\$3) and (logic with configur\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:30
S17 0	3	(loopback with output with result) and (fail\$3 with indicat\$3) and (logic with configur\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:50
S17 1	3	(loopback with output with result) and (logic with configur\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:56
S17 2	1	(loopback with output with indicator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 16:00
S17 4	37	(loopback with failure with indicat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:02

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S17 6	4	(loopback with failure with indicat\$3) and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 16:02
S17 8	1	((inverse with routing) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:20
S17 9	52	((inverse with routing) and ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:33
S18 0	4	((inverse adj routing) and ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:33

DA

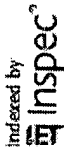


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| #1 | (configurable logic block<and>verifier)<and>failure indicator | Results |
| #2 | (testing routing<and>input data)<and>inverse configuration | 0 |



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